Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A bus clock controlling method in a computer, comprising:

setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a CPU and a controlling device;

detecting a remaining battery capacity if a present power source is at least one battery; and

adjusting the set throttle rate according to the detected remaining battery capacity.

2. (Original) The method set forth in claim 1, wherein said adjusting step increases the set throttle rate as the detected remaining battery capacity decreases.

3. (Original) The method set forth in claim 1, wherein said adjusting step selects one value appropriate to the detected remaining battery capacity among a plurality of throttle rates preset in reverse proportion to different remaining battery capacities.

4. (Original) The method set forth in claim 1, wherein said controlling device is a bridge controller in a computer.

5. (Original) A bus clock controlling method in a computer, comprising:

setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a CPU and a controlling device;

detecting a present load of the CPU; and

adjusting the set throttle rate in reverse proportion to the present CPU load.

6. (Original) The method set forth in claim 5, wherein said adjusting step is conducted only when a present power source is at least one battery.

7. (Original) The method set forth in claim 5, wherein said adjusting step includes selecting a new throttle rate appropriate to the detected CPU load from a plurality of throttle rates preset in reverse proportion to different CPU loads.

8. (Original) A computer, comprising:

a CPU that processes;

a first controller coupled to the CPU via a data bus, and configured to provide a throttled clock to the data bus according to a throttle rate;

a clock generator coupled to the CPU and the first controller, and configured to generate a clock;

a detector detecting a variable, wherein the variable is a remaining battery capacity or a load of the CPU; and

a second controller coupled to receive the detected variable, configured to determine the throttle rate according to the detected variable, and further configured to output the throttle rate to the first controller.

9. (Original) The computer of claim 8, wherein said second controller outputs the throttle rate in the form of a pulse signal whose duty cycle varies in accordance with the detected variable, and wherein the first controller includes a throttle controller providing the data bus with the throttled clock only when the pulse signal is in a specific state.

10. (Original) The computer of claim 8, wherein said first controller is a bridge controller, and wherein said second controller determines the throttle rate in reverse proportion to the detected variable.

11. (Original) The computer of claim 8, wherein the throttle rate increases as a value of the detected variable decreases.

12. (Original) The computer of claim 8, wherein the second controller comprises:

at least one comparator coupled to receive the detected variable from the detector, configured to compare the detected variable to a plurality of predetermined values, and further configured to output a result of the corresponding plurality of comparisons; and

a host clock throttler coupled to receive the plurality of comparisons and a power mode signal, and configured to output the throttle rate to the first controller.

13. (Original) The computer of claim 12, wherein the at least one comparator comprises a remaining battery capacity comparator, and wherein the detected variable is the remaining battery capacity.

14. (Original) The computer of claim 12, wherein the at least one comparator comprises a CPU load comparator, and wherein the detected variable is the load of the CPU.

15. (Original) The computer of claim 12, wherein the at least one comparator comprises a remaining battery capacity comparator and a CPU load comparator.

16. (Original) A bus clock controlling method in a computer, comprising:

setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus to which both a CPU and a controlling device are connected;

detecting a remaining battery capacity and a load of the CPU if a present power source is a battery; and

adjusting the set throttle rate according to the detected remaining battery capacity and the CPU load.

17. (Currently Amended) A bus clock controlling method in a portable computer, comprising:

setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus connected between a controlling device and a selected one of a plurality of devices associated with the portable computer;

detecting a condition of a ~~prescribed criteria~~ remaining battery or a CPU load of the portable computer if a present power source is a battery; and

adjusting the set throttle rate according to the detected condition, wherein the detected condition is within a range of values for the prescribed criteria.

18. (Original) The bus clock controlling method of claim 17, wherein the selected device is a peripheral device, and wherein the predetermined initial value is a smallest throttle rate.

19. (Currently Amended) The bus clock controlling method of claim 17, wherein ~~the prescribed criteria is at least one of CPU load and remaining battery capacity, and wherein~~ said adjusting step selects a rate corresponding to the detected condition among a plurality of prescribed throttle rates that each correspond to mutually exclusive sets of values of the detected condition within the range of values for the prescribed criteria.

20. (Original) The bus clock controlling method of claim 19, wherein each of the plurality of prescribed throttle rates increases as the detected condition decreases within the range.

21. (Original) A bus clock controlling method in a computer, comprising

setting a throttle rate of a clock to a predetermined initial value, the clock being used for a data bus to which both a controlling device and a peripheral device are connected;

detecting one of a present load of the CPU and a remaining battery capacity; and

adjusting the set throttle rate in reverse proportion to the detected one of the present CPU load and the remaining battery capacity.

22. (Canceled)

23. (New) The method of claim 1, comprising:

generating a second clock for the CPU and the controlling device; and

determining the throttle rate using a second controlling device according to the remaining battery capacity and outputting the throttle rate to the controlling device, wherein said second controlling device outputs the throttle rate in the form of a pulse signal whose duty cycle varies in accordance with the detected remaining battery capacity, and wherein the controlling device includes a throttle controller providing the data bus with the throttled clock only when the pulse signal is in a specific state.

24. (New) The method of claim 5, comprising:

generating a second clock for the CPU and the controlling device; and

determining the throttle rate using a second controller according to the remaining battery capacity and outputting the throttle rate to the controlling device, wherein said second controller outputs the throttle rate in the form of a pulse signal whose duty cycle varies in accordance with the present load of the CPU, and wherein the controlling device includes a throttle controller providing the data bus with the throttled clock only when the pulse signal is in a specific state.

25. (New) The method of claim 21, comprising:

generating a second clock for the CPU and the controlling device; and

determining the throttle rate using a second controller according to the remaining battery capacity and outputting the throttle rate to the controlling device, wherein said second controller outputs the throttle rate in the form of a pulse signal whose duty cycle varies in accordance with the detected one of the present CPU load and the remaining battery capacity, and wherein the controlling device includes a throttle controller providing the data bus with the throttled clock only when the pulse signal is in a specific state.